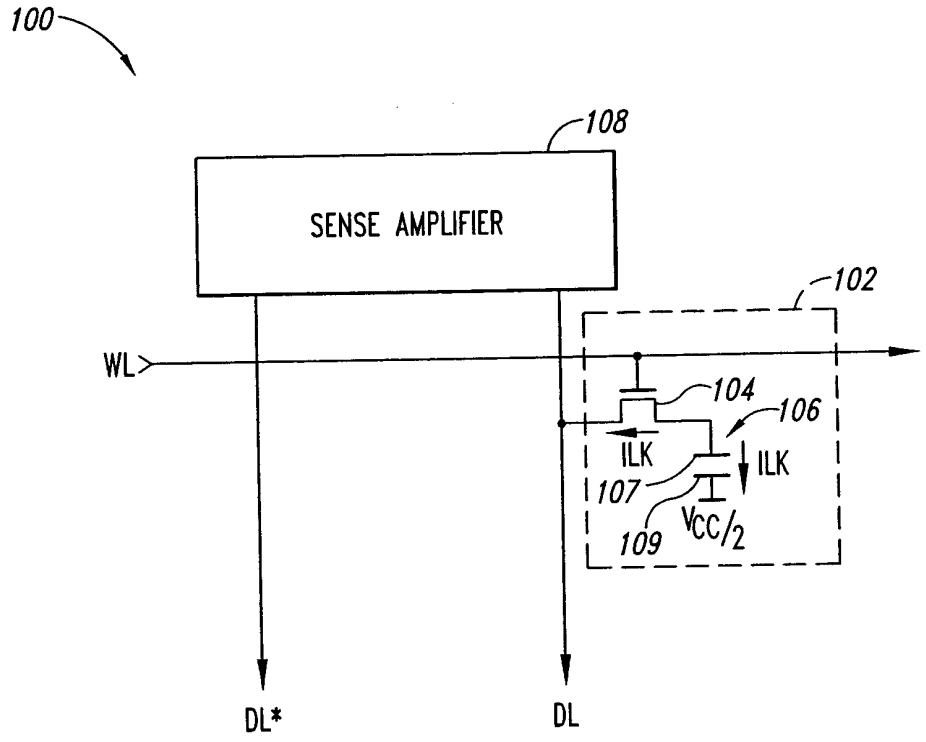

Fig. 1
(Background Art)

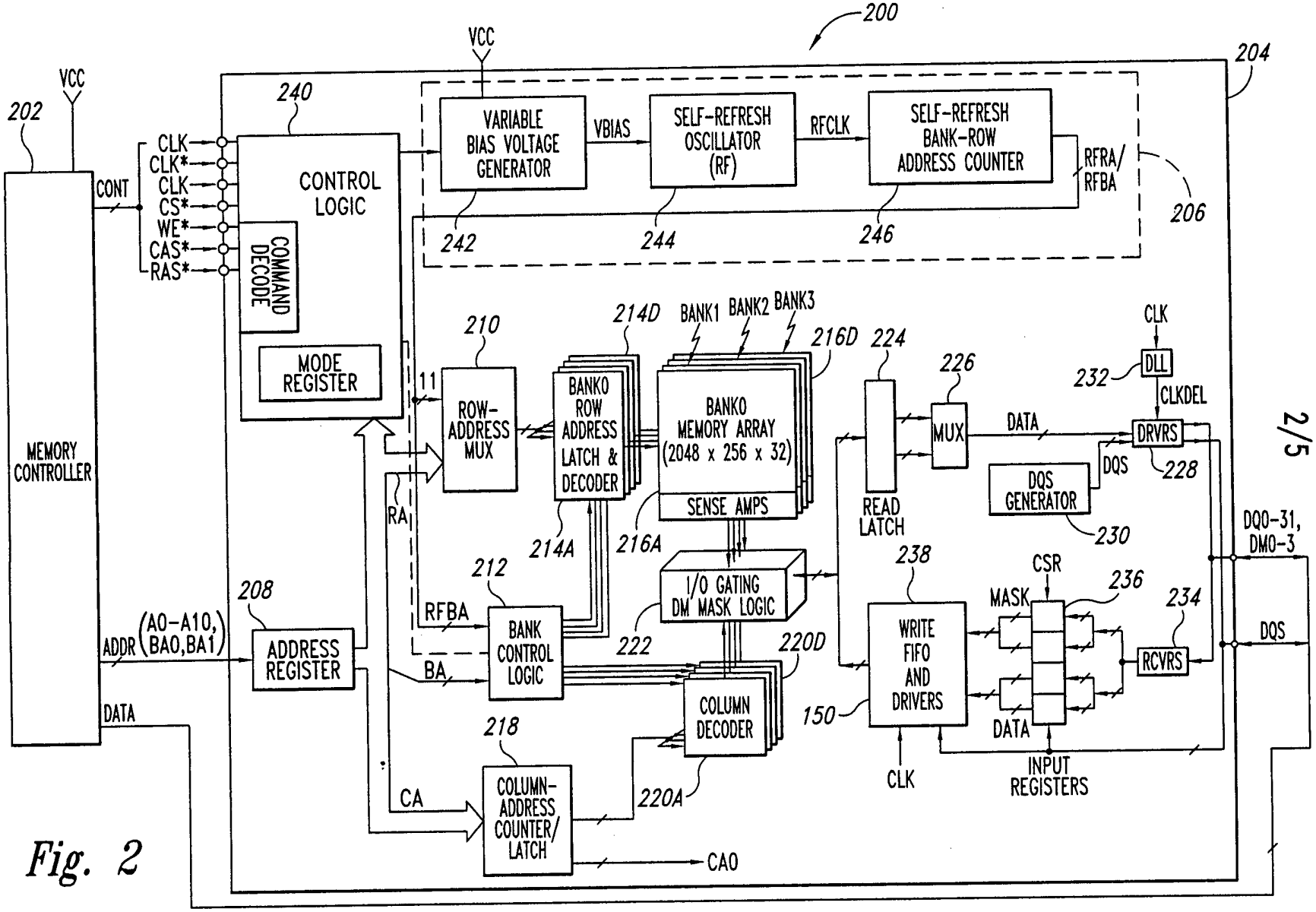
200
VCC
202
204
240
VARIABLE BIAS VOLTAGE GENERATOR
VBIAS
SELF-REFRESH OSCILLATOR (RF)
RFCLK
SELF-REFRESH BANK-ROW ADDRESS COUNTER
RFRA/ RFBA
206
242
244
246
CLK
CLK*
CLK
CS*
WE*
CAS*
RAS*
CONT
CONTROL LOGIC
COMMAND DECODE
MODE REGISTER
MEMORY CONTROLLER
210
214D
BANK1
BANK2
BANK3
216D
224
226
CLK
232
DLL
CLKDEL
11
ROW-ADDRESS MUX
BANK0 ROW ADDRESS LATCH & DECODER
BANK0 MEMORY ARRAY (2048 x 256 x 32)
SENSE AMPS
READ LATCH
MUX
DATA
DRVRS
DQS
228
DQS GENERATOR
230
DQ0-31, DM0-3
RA
214A
216A
212
I/O GATING DM MASK LOGIC
238
CSR
MASK
236
234
RFBA
BANK CONTROL LOGIC
222
220D
WRITE FIFO AND DRIVERS
RCVRS
DQS
208
ADDR
(A0-A10, BA0,BA1)
ADDRESS REGISTER
BA
COLUMN DECODER
150
DATA
218
CLK
INPUT REGISTERS
DATA
COLUMN-ADDRESS COUNTER/ LATCH
CA
220A
CA0

Fig. 2

2/5

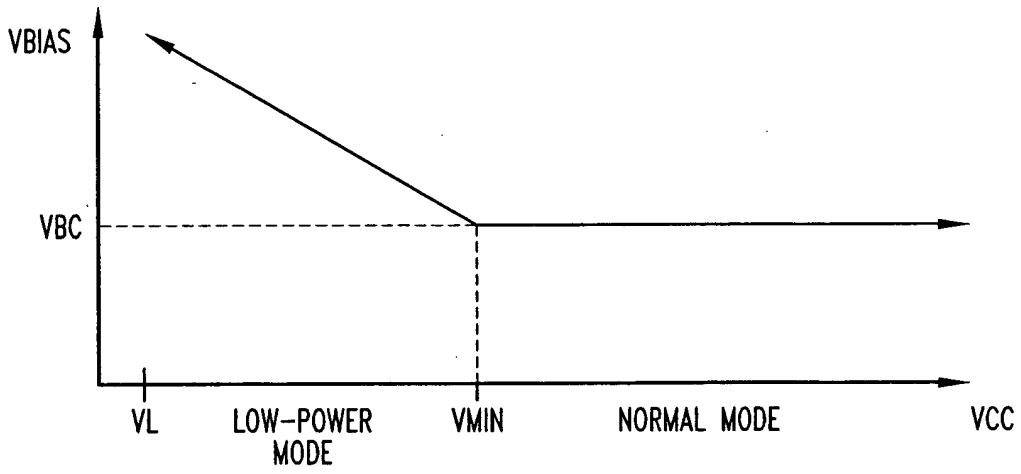
VBIAS
VBC
VL
LOW-POWER MODE
VMIN
NORMAL MODE
VCC

Fig. 3A

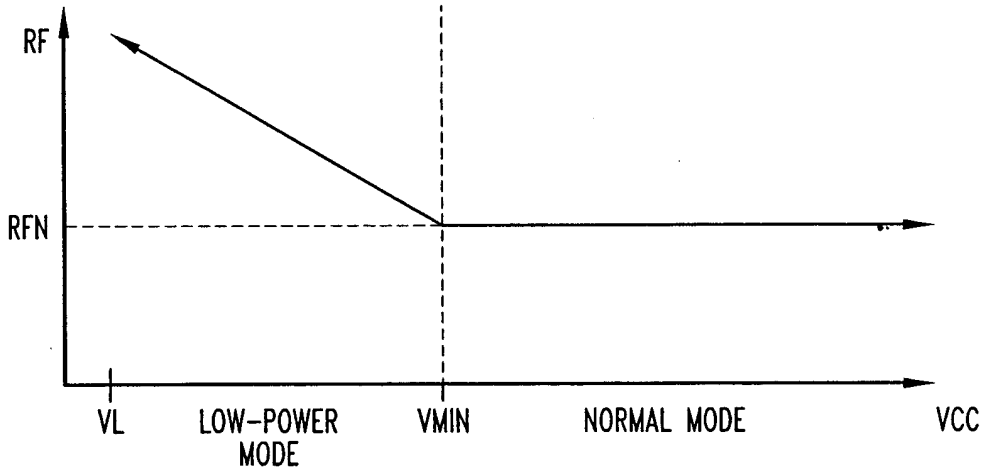
RF
RFN
VL
LOW-POWER MODE
VMIN
NORMAL MODE
VCC

Fig. 3B

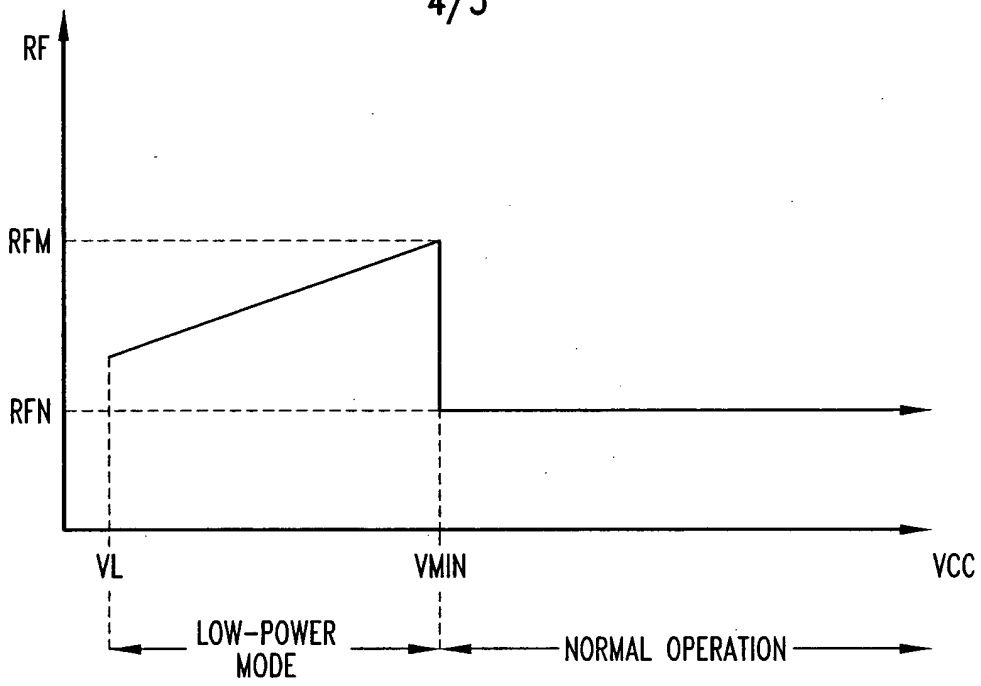
RF
RFM
RFN
VL
VMIN
VCC
LOW-POWER MODE
NORMAL OPERATION

Fig. 4

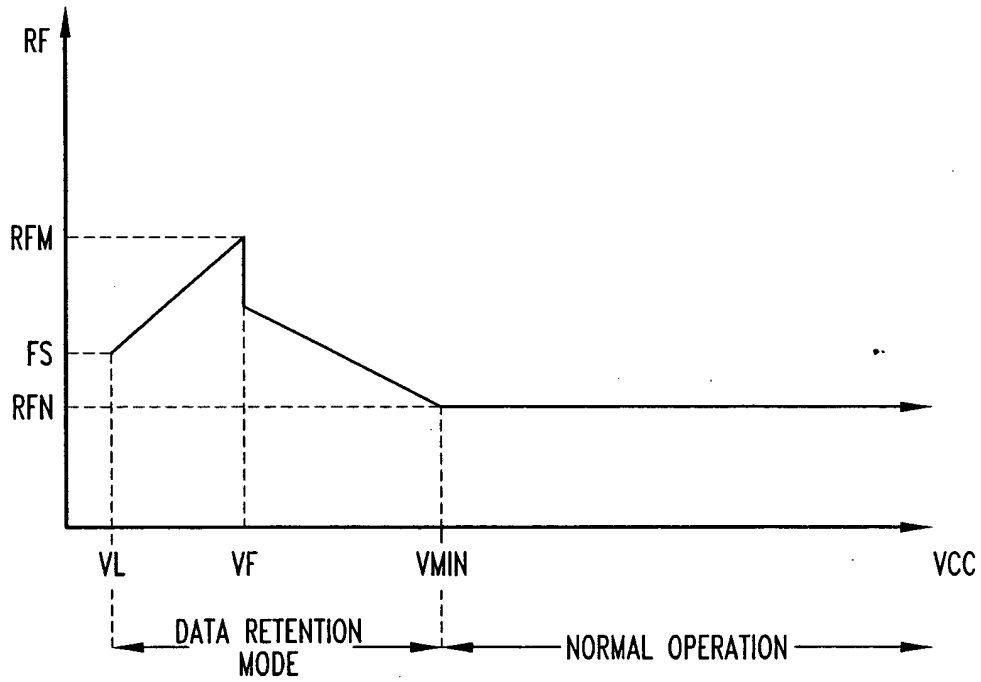
RF
RFM
FS
RFN
VL
VF
VMIN
VCC
DATA RETENTION MODE
NORMAL OPERATION

Fig. 5

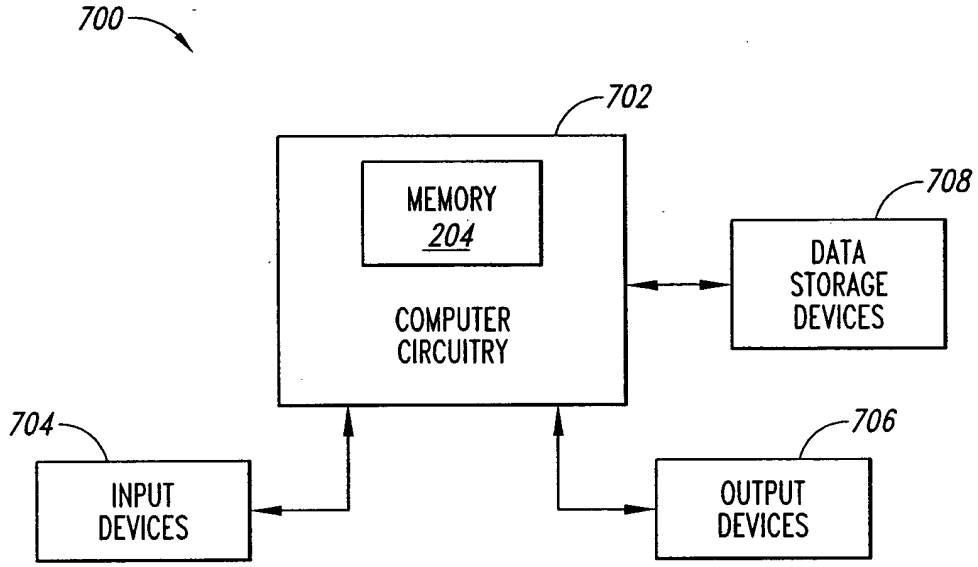
700
702
MEMORY
204
COMPUTER
CIRCUITRY
708
DATA
STORAGE
DEVICES
704
INPUT
DEVICES
706
OUTPUT
DEVICES

Fig. 6